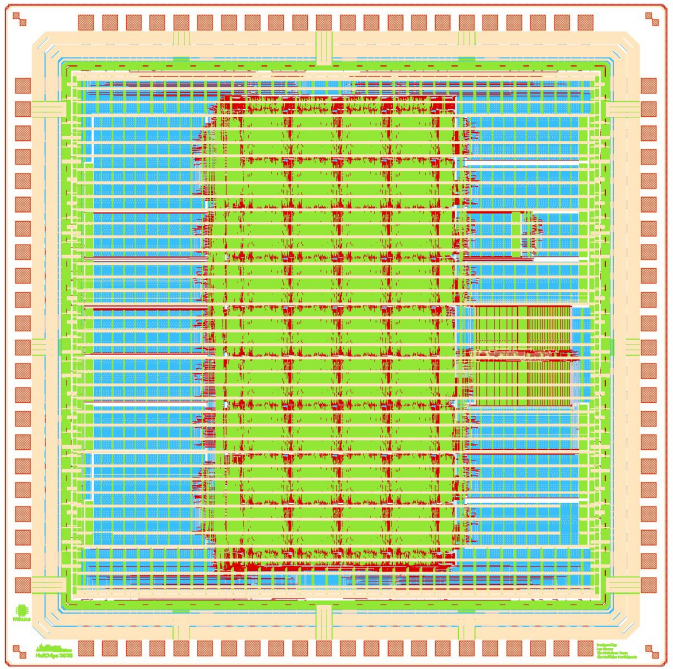
Hackathon Intro

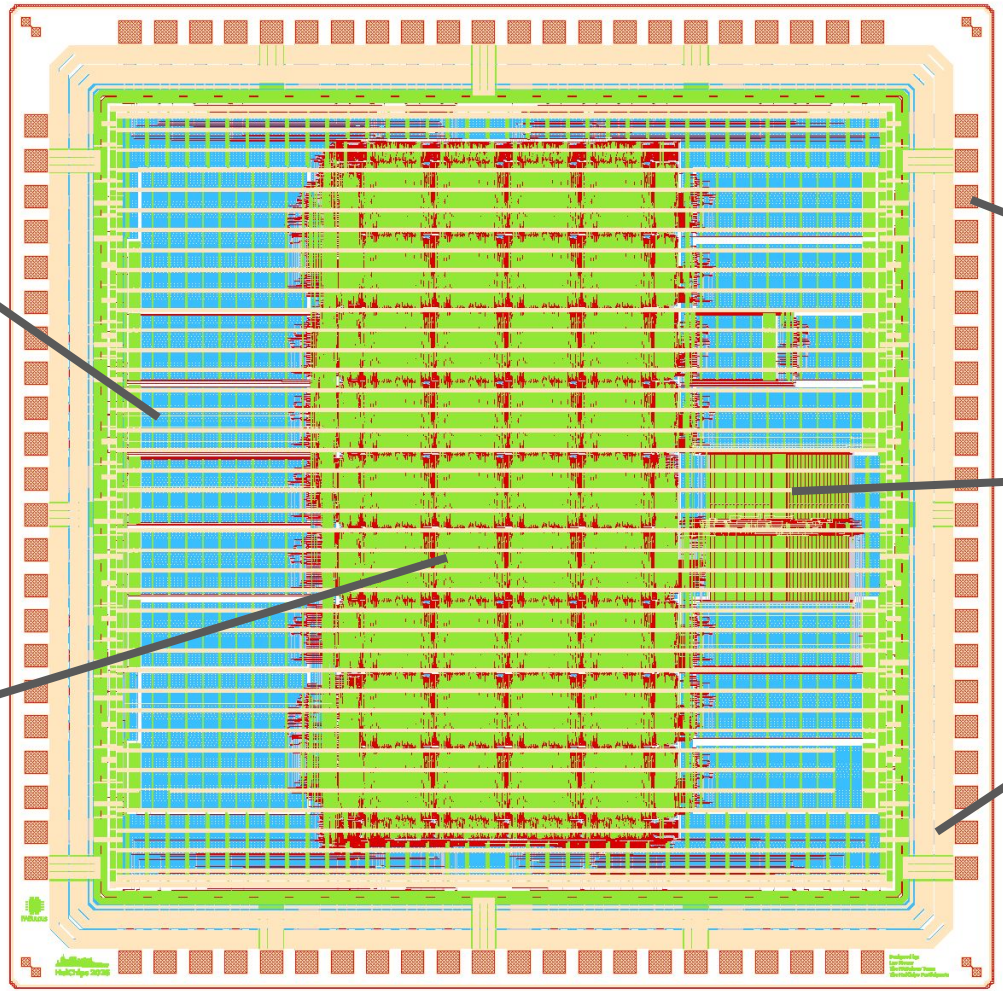
Leo Moser

HeiChips 2026 Tapeout!

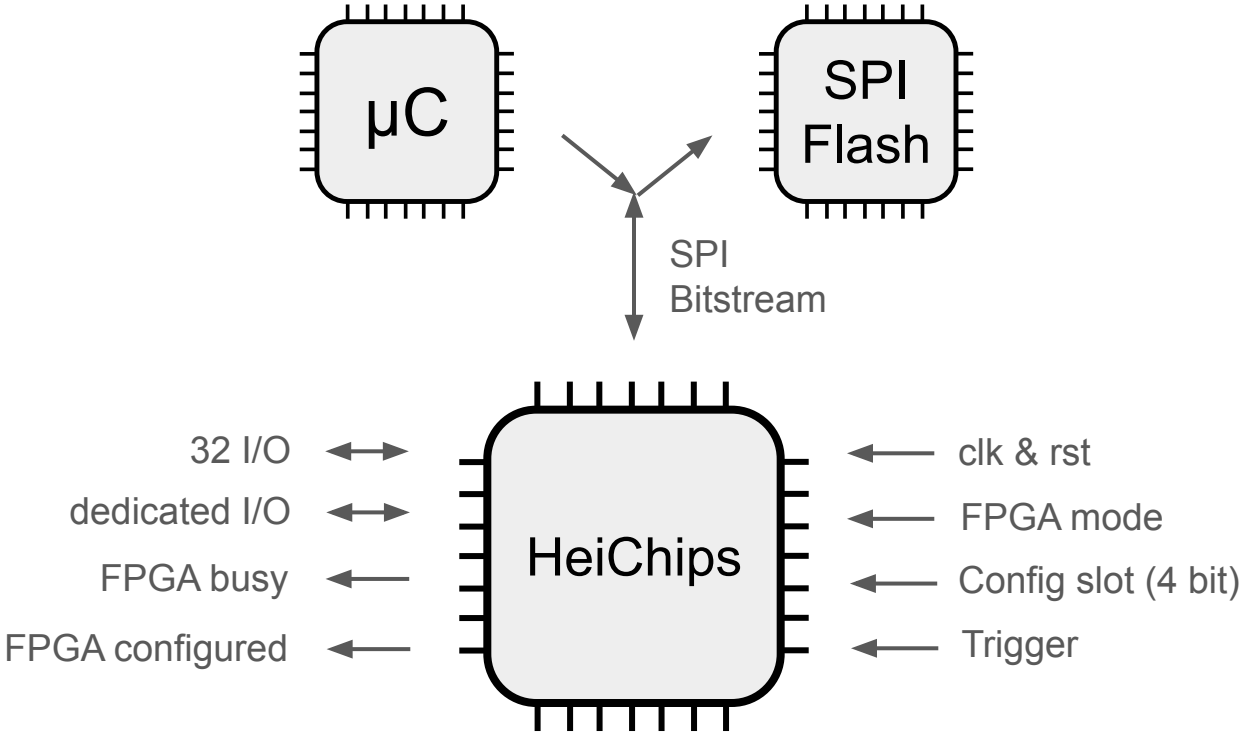
- IHP Open PDK - SG13CMOS5L
- Embedded FPGA in the center
- 32 slots available
- User Projects
  - Tiny: 1 slot
  - Small: 2 slots
  - Large: 4 slots
- 4 KiB SRAM
- Repository:
  - https://github.com/HeiChips/heichips26-tapeout



HeiChips 2026 Tapeout


User Project
Bondpad
SRAM
eFPGA
Pad ring

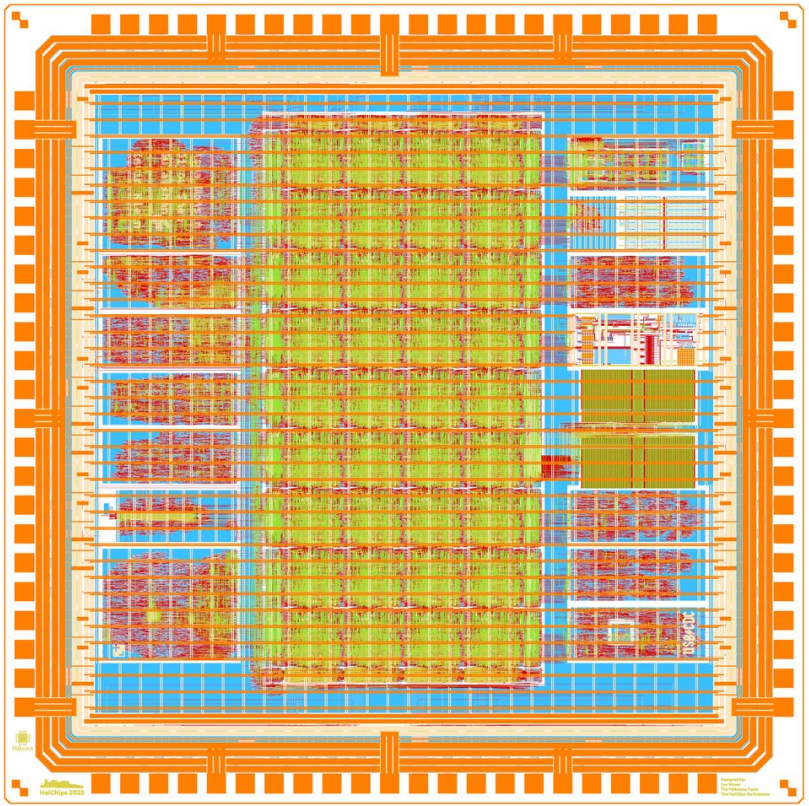
Chip I/Os

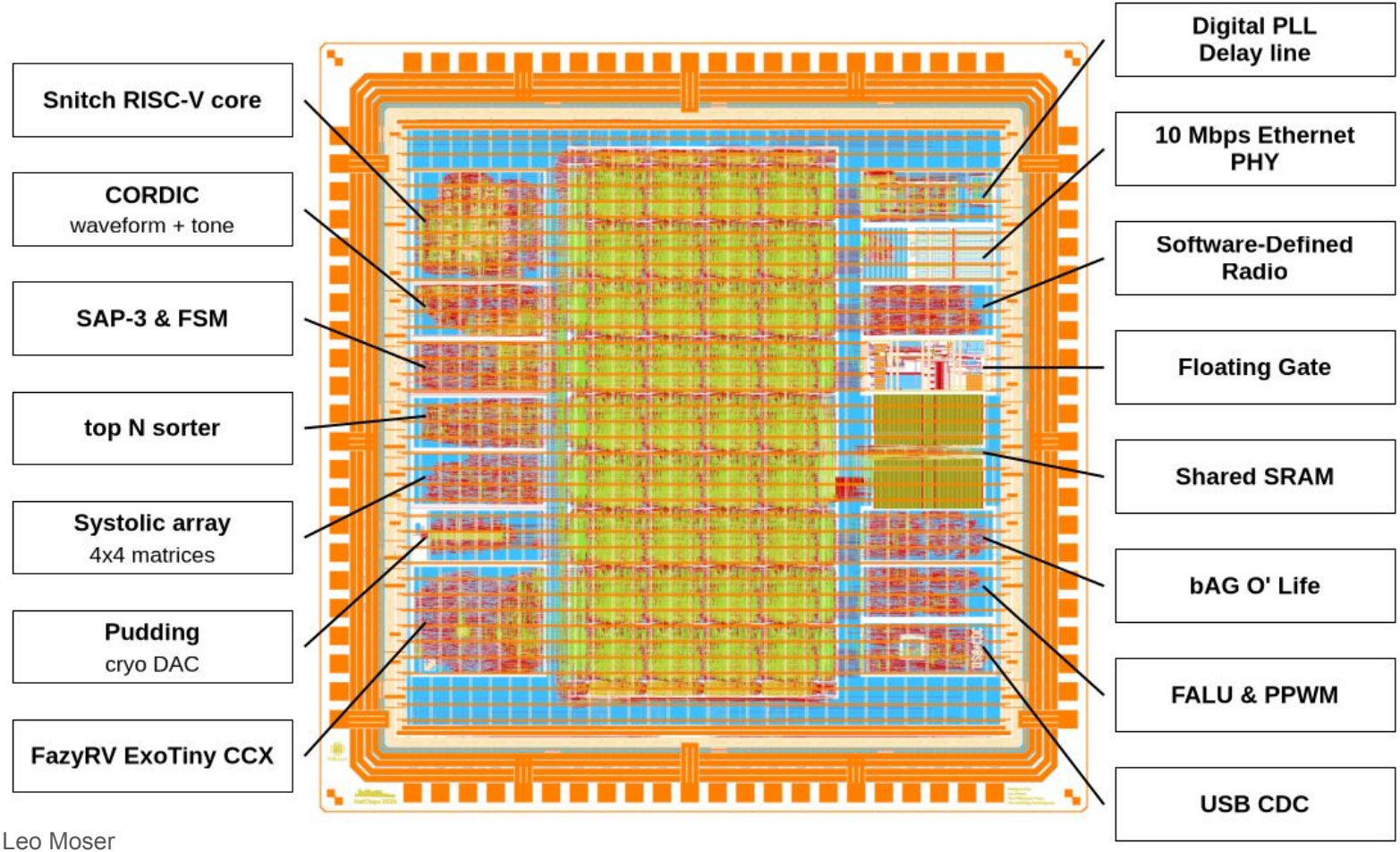

µC
SPI Flash
SPI
Bitstream
HeiChips
32 I/O
dedicated I/O
FPGA busy
FPGA configured
clk & rst
FPGA mode
Config slot (4 bit)
Trigger

What about last year?

HeiChips 2025 Tapeout

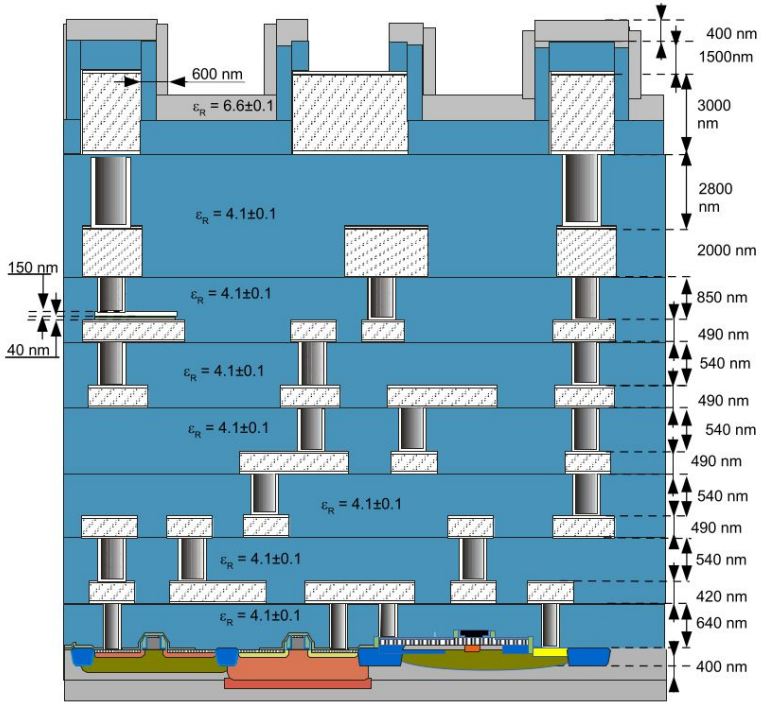
- 9 mm², IHP SG13G2
- FABulous eFPGA
  - 32x I/Os
  - 288x LUT4 + FF
  - 1x SRAM (4 KiB)
  - 4x global buffers
  - 1x system reset
- User projects can connect to:
  - I/Os
  - each other
  - SRAM



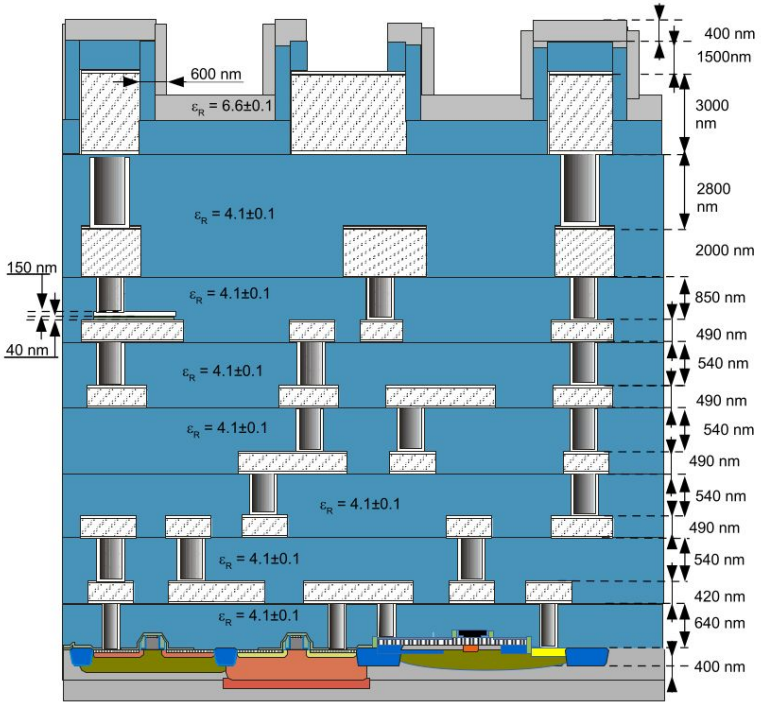

Snitch RISC-V core
CORDIC
waveform + tone
SAP-3 & FSM
top N sorter
Systolic array
4x4 matrices
Pudding
cryo DAC
FazyRV ExoTiny CCX
Digital PLL
Delay line
10 Mbps Ethernet
PHY
Software-Defined
Radio
Floating Gate
Shared SRAM
bAG O' Life
FALU & PPWM
USB CDC

New Manufacturing Process

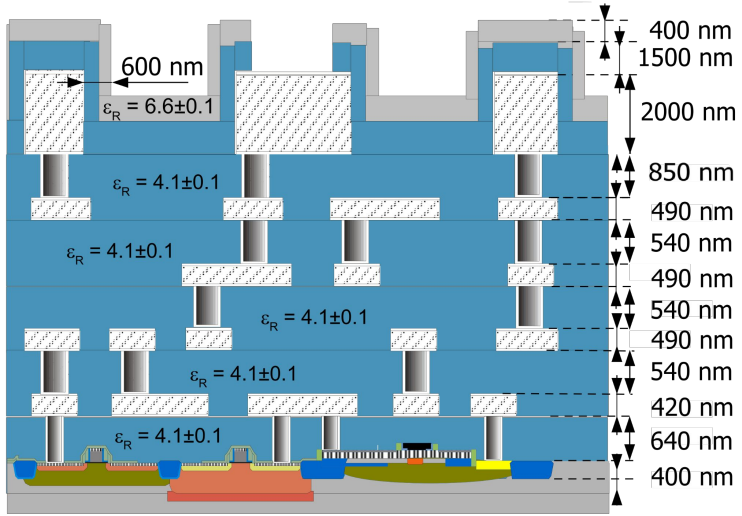
SG13G2 Process Cross Section



SG13G2



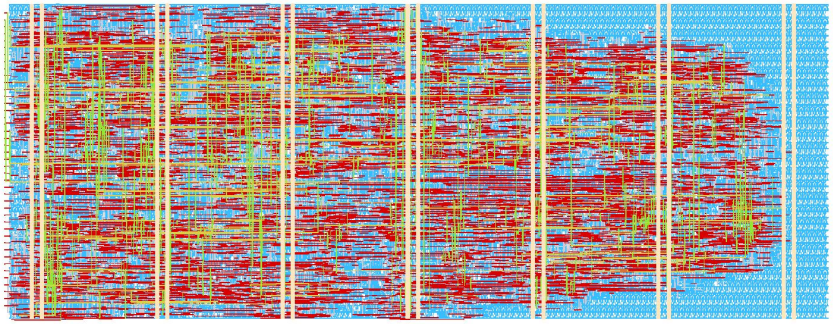
SG13CMOS5L



Power Gating

HeiChips25: No Power Gating!

- What if there’s a short?
- We could ask participants to run LVS?
- We want to take any GDS!



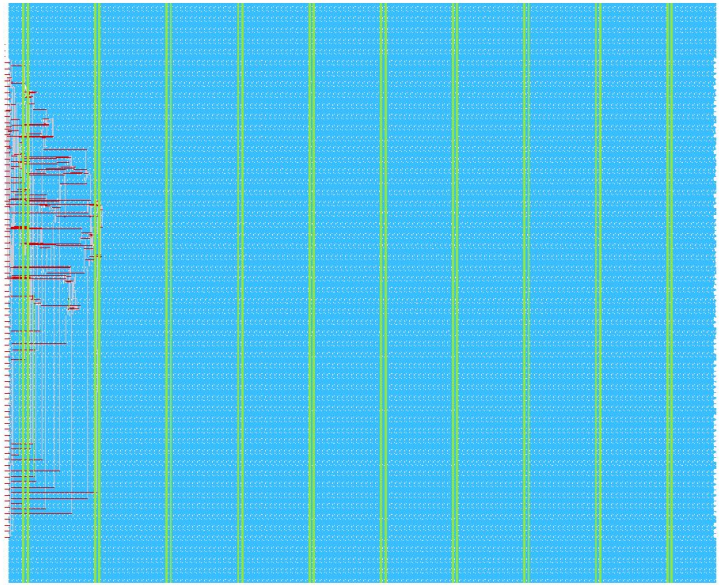
Solution: Power Gates

HeiChips26: Power Gates + VAPWR

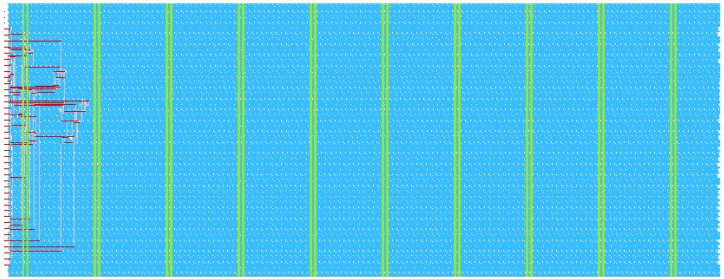
- Every project is power gated (digital and analog)
  - Thanks Daniel!
- In addition to the digital power rail (VPWR), you can use an analog power rail (VAPWR).
- Still to be determined:
  - IOVDD or separate analog domain? No promises yet!

Project Templates!

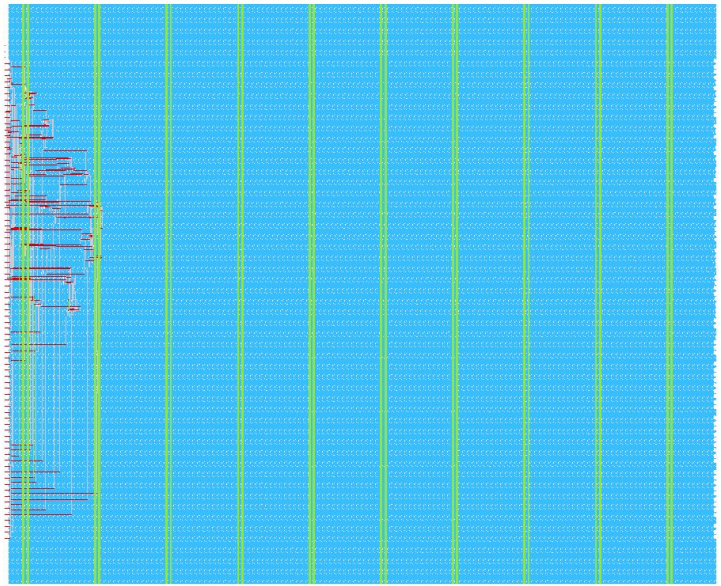
Large



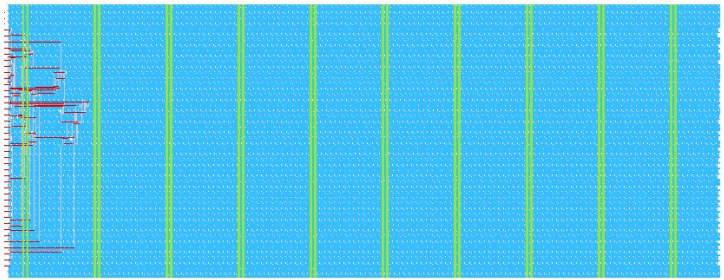
Small

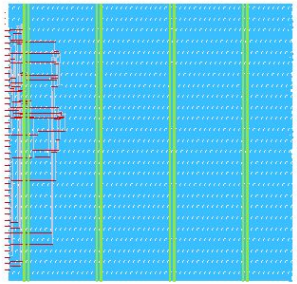


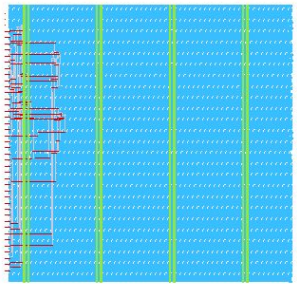
Large



Small







Tiny

Tiny

Project Templates

- **Tiny** project template: **200** µm × **200** µm
- **Small** project template: **500** µm × **200** µm
- **Large** project template: **500** µm × **415** µm

- Chip provides 32 slots
  - Large: 4 slots
  - Small: 2 slots
  - Tiny: 1 slot

- Chip has 18 unused I/Os
  - direct connection to pads
  - up to 3 analog pins per project

Digital Interface

- Same interface as Tiny Tapeout
  - clock, reset, 8 inputs, 8 outputs, 8 bidirectional I/Os
- Large projects have double I/Os:
  - clock, reset, 16 inputs, 16 outputs, 16 bidirectional I/Os
- Connects to the I/O pads through the eFPGA fabric

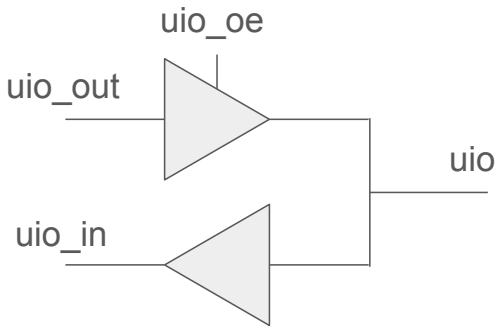
- Need dedicated pins?
  - High-speed digital
  - Analog mixed-signal

→ **come and talk to us!**

Tiny Tapeout Pinout

- Pinout
  - 10 input pins — clk, rst, 8x ui_in
  - 8 output pins — 8x uo_out
  - 8 bidirectional pins — 8x uio_in, 8x uio_out, 8x uio_oe
  - always 1 — ena (just ignore it)
- Common pin assignment
  - Makes it easier to test other designs
  - https://tinytapeout.com/specs/pinouts
- Standardized Pmods
  - VGA, QSPI, Audio etc.
  - You can buy them: https://store.tinytapeout.com

```
module heichips26_template (
    input  wire [7:0] ui_in,
    output wire [7:0] uo_out,
    input  wire [7:0] uio_in,
    output wire [7:0] uio_out,
    output wire [7:0] uio_oe,
    input  wire       ena,
    input  wire       clk,
    input  wire       rst_n
);
```



Tool Setup!

Installation of the Tools

- Using Nix
  - Native Installation: Linux (x86_64, aarch64) and macOS (x86_64, arm64)
  - Windows: Emulation (e.g. WSL2)
  - Based on: [fossi-foundation/nix-eda]
- Follow the installation instructions in the workshop repositories
- To enable the tools:
  - Run: `nix-shell`
- For openXC7 Toolchain
  - `cd nix-openxc7 && nix-shell`

Simulation & Verification

Simulators

- Icarus Verilog
- Verilator

Testbench environment

- cocotb
  - Python-based
  - simulator-agnostic
  - Easy to use :)

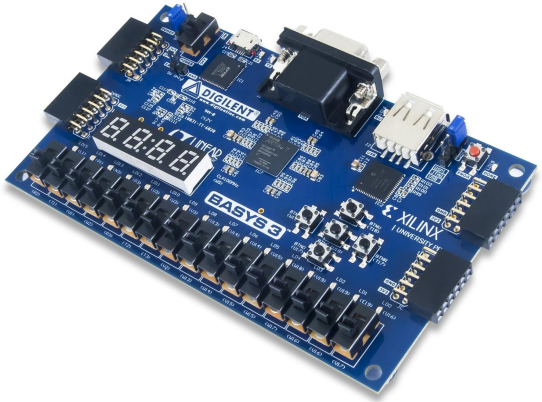
FPGA Prototyping

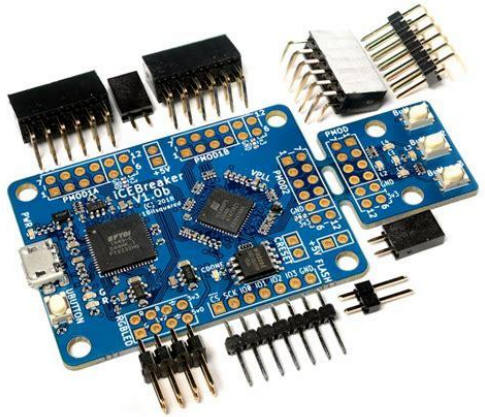
Open Source Toolchain

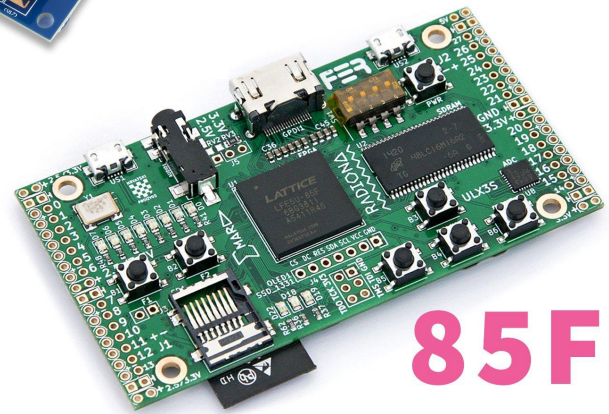
- Yosys - synthesis tool
- nextpnr - place and route
- openFPGALoader

Supported Boards

- iCEBreaker
- ULX3S
- Basys 3
- …







Analog Design

Schematic Entry

- Xschem

Analog Simulation

- Ngspice

Layout Entry

- KLayout

LVS and DRC

- KLayout
- magic + netgen

Now it's your move:

Think about your project ideas!